In the Specification:

Amend the specification as follows:

First numbered page, line 1, before "Background of the Invention" insert the following as a separate paragraph:

--This is a divisional of co-pending application serial no. 08/771,581, filed 12/20/96, entitled "A Method and Apparatus for a Fault Tolerant, Software Transparent and High Data Integrity Extension to a Backplane Bus or Interconnect" by the same inventor, which is incorporated herein by reference in its entirety.--

In the Claims:

Please cancel, without prejudice, the claims: 1-90.

Claims 91-98 are unchanged and provided below for the Examiner's convenience:

91. (unchanged) A method for automatically constructing a routing tag for a cell based on an address provided by a bus operation on a bus connected to a first node of a system interconnect comprising the steps of:

(a) capturing said address from said bus; and

(b) converting said address into a value stored in said routing tag.

92. (unchanged) The method of claim 91 wherein step (b) further comprises:

(b1) accessing said value from a first address mapping content addressable memory (fAMCAM) after assertion of said address to said fAMCAM.

93. (unchanged) The method of claim 92 wherein said fAMCAM comprises a first register that defines an address window on said bus.

94. (unchanged) The method of claim 93 wherein said system interconnect further comprises a second node with a second address mapping content addressable memory (sAMCAM) and a second register, and said method further comprises:

(c) storing a configuration value in said first register; and

(d) broadcasting said configuration value to said second node for storage in said second register.

95. (unchanged) An apparatus for automatically constructing a routing tag for a cell based on an address provided by a bus operation on a bus connected to a first node of a system interconnect comprising:

an address capturing mechanism configured to capture said address from said bus; and

an address conversion mechanism configured to convert said address from said bus into a value stored in said routing tag of said cell.

96. (unchanged) The apparatus of claim 95 wherein the address conversion mechanism further comprises:

a first address mapping content addressable memory (fAMCAM) configured to produce said value after assertion of said address to said fAMCAM.

97. (unchanged) The apparatus of claim 96 wherein said fAMCAM comprises a first register that defines an address window on said bus.

98. (unchanged) The apparatus of claim 97 wherein said system interconnect further comprises a second node with a second address mapping content-addressable memory (sAMCAM) and a second register and said apparatus further comprises:

a storage mechanism configured to store a configuration value in said first register; and

a broadcast mechanism configured to broadcast said configuration value to said second node for storage in said second register.

Please add the following new claims 99-154:

99. (new) The method of claim 91 further comprising steps of:

detecting an interrupt condition change at said first node, said interrupt condition change comprising either an interrupt assertion or an interrupt deassertion;

creating an interrupt cell at said first node responsive to the detecting said interrupt condition change, said interrupt cell addressed to a second node and containing said interrupt condition change;

transporting said interrupt cell to said second node; and

asserting an interrupt signal at said second node responsive to said interrupt condition change.

100. (new) The method of claim 99 wherein the step of asserting further comprises steps of:

recognizing said interrupt cell containing said interrupt assertion at said second node; and

incrementing an up/down counter.

101. (new) The method of claim 100 wherein the step of asserting further comprises steps of:

detecting that said up/down counter is non-zero; and

posting an interrupt at said second node.

102. (new) The method of claim 99 wherein said cell further comprises a first node identifier and the step of asserting further comprises:

saving said first node identifier and said interrupt condition change.

103. (new) The method of claim 99 wherein the step of asserting further comprises steps of:

recognizing said interrupt cell containing said interrupt deassertion; and

decrementing an up/down counter.

104. (new) The method of claim 103 wherein the step of asserting further comprises steps of:

detecting that said up/down counter is zero; and

clearing an interrupt at said second node.

105. (new) The method of claim 99 wherein said interrupt cell comprises an interrupt security code and the step of asserting further comprises matching said interrupt security code with a second node interrupt security code.

106. (new) The method of claim 99 wherein said interrupt condition is a result of a bus error on said bus.

107. (new) The method of claim 106 wherein said bus is a PCI bus and said bus error results in a SERR assertion.

108. (new) The method of claim 94 wherein said sAMCAM uses said configuration value to configure itself.

109. (new) The method of claim 108 wherein said second register defines a second address window on a second bus.

110. (new) The method of claim 93 wherein said bus is a PCI bus and said first register is selected from the group of an input/output limit register, input/output base register, a memory limit register, a memory base register, a prefetchable memory limit register, a prefetchable memory base register, an input/output limit upper register, and an input/output base upper register or a secondary bus number register.

111. (new) The method of claim 91 wherein said address is of a control status register (CSR) of a device attached to a second bus itself attached to said system interconnect by a second node, said method further comprising steps of:

(c) broadcasting said cell over said system interconnect;

(d) receiving said cell by said second node;

(e) accessing said CSR; and

(f) sending, by said second node, a response cell to said first node.

112. (new) The method of claim 91 wherein said bus is a PCI bus.

113. (new) The method of claim 91 further comprising steps of:

generating at least one transfer attribute from said bus operation; and

including said at least one transfer attribute within said cell.

114. (new) The method of claim 91 wherein said cell is a read-initiate cell, an interrupt transition cell, a read response cell, a write-initiate cell, or a write-response cell.

115. (new) The method of claim 91 wherein said cell includes a cache line.

116. (new) The method of claim 92 further comprising:

automatically initializing said fAMCAM responsive to one or more operations on said bus.

117. (new) The method of claim 116 wherein said bus is a PCI bus and said operations are type 1 control status register (CSR) cycles on said PCI bus.

118. (new) The method of claim 91 further comprising maintaining at least one incomplete transaction cache (ITC).

119. (new) The method of claim 118 wherein said ITC includes a sliding window having a width, said method further comprising steps of:

delaying transmission of said cell responsive to a reduction of said width; and

resuming transmission of said cell responsive to an increase of said width.

120. (new) The method of claim 118 wherein said ITC includes a sliding window having a width, said method further comprising adjusting said width responsive to said first node receiving said cell or a response cell.

121. (new) The method of claim 91 wherein said first node is a host node, and said method further comprising steps of:

determining whether said value identifies said host node; and

broadcasting said cell dependent on the step of determining when said value does not identify said host node.

122. (new) The method of claim 91 further comprising steps of:

converting said bus operation into said cell;

transporting said cell over said system interconnect from said first node to a second node; and

performing an equivalent bus operation on a second bus by said second node after receipt of said cell by said second node.

123. (new) The method of claim 122 wherein said first bus is a first PCI bus and said second bus is a second PCI bus.

124. (new) The method of claim 122 wherein said first bus is a PCI bus and said second bus is not.

125. (new) The method of claim 122 further comprising steps of:

creating a second cell containing status of said equivalent bus operation;

transporting said second cell to said first node;

completing said bus operation upon receipt of said second cell.

126. (new) The method of claim 122 wherein the step of converting includes steps of:

determining, responsive to said bus operation, an identifier for said second node from an address mapping content addressable memory (AMCAM); and

including said identifier in said cell.

127. (new) The apparatus of claim 95 further comprising:

an interrupt detection mechanism configured to detect an interrupt condition change at said first node, said interrupt condition change comprising either an interrupt assertion or an interrupt deassertion;

an interrupt cell creation mechanism configured to create an interrupt cell at said first node responsive to the interrupt detection mechanism, said interrupt cell being addressed to a second node and containing said interrupt condition change;

a cell transportation mechanism configured to transport said interrupt cell to said second node; and

an interrupt assertion mechanism configured to assert an interrupt signal at said second node responsive to said interrupt condition change.

128. (new) The apparatus of claim 127 wherein the interrupt assertion mechanism further comprises:

an interrupt assertion recognition mechanism at said second node configured to recognize said interrupt cell containing said interrupt assertion and increment an up/down counter.

129. (new) The apparatus of claim 128 wherein the interrupt assertion mechanism further comprises:

a post interrupt mechanism configured to detect that said up/down counter is non-zero and to post an interrupt at said second node.

130. (new) The apparatus of claim 127 wherein said cell further comprises a first node identifier and the interrupt assertion mechanism further comprises:

a storage mechanism configured to save said first node identifier and said interrupt condition change.

131. (new) The apparatus of claim 127 wherein the interrupt assertion mechanism further comprises:

an interrupt deassertion recognition mechanism at said second node configured to recognize said interrupt cell containing said interrupt deassertion, and decrement an up/down counter.

132. (new) The apparatus of claim 110 wherein the interrupt assertion mechanism further comprises:

a clear interrupt mechanism configured to detect that said up/down counter is zero and to clear an interrupt at said second node.

133. (new) The apparatus of claim 127 wherein said interrupt cell comprises an interrupt security code and the interrupt assertion mechanism further comprises:

an interrupt security mechanism configured to match said interrupt security code with a second node interrupt security code.

134. (new) The apparatus of claim 127 wherein said interrupt condition is a result of a bus error on said bus.

135. (new) The apparatus of claim 134 wherein said bus is a PCI bus and said bus error results in a SERR assertion.

136. (new) The apparatus of claim 98 wherein said sAMCAM uses said configuration value to configure itself.

137. (new) The apparatus of claim 136 wherein said second register defines a second address window on a second bus.

138. (new) The apparatus of claim 97 wherein said bus is a PCI bus and said first register is selected from the group of an input/output limit register, input/output base register, a memory limit register, a memory base register, a prefetchable memory limit register, a prefetchable memory base register, an input/output limit upper register, and an input/output base upper register or a secondary bus number register.

139. (new) The apparatus of claim 95 wherein said address is of a control status register (CSR) of a device attached to a second bus itself attached to said system interconnect by a second node, said apparatus further comprising:

a broadcast mechanism configured to broadcast said cell over said system interconnect from said first node;

a reception mechanism at said second node configured to receive said cell;

a bus operation mechanism in said second node configured to access said CSR over said second bus; and

a response mechanism in said second node configured to send a response cell to said first node.

140. (new) The apparatus of claim 95 further wherein said bus is a PCI bus.

141. (new) The apparatus of claim 95 further comprising:

a transfer attribute generation mechanism configured to generate at least one transfer attribute from said bus operation for inclusion within said cell.

142. (new) The apparatus of claim 95 wherein said cell is a read-initiate cell, an interrupt transition cell, a read response cell, a write-initiate cell, or a write-response cell.

143. (new) The apparatus of claim 95 wherein said cell includes a cache line.

144. (new) The apparatus of claim 96 further comprising:

an initialization mechanism configured to automatically initialize said fAMCAM responsive to one or more operations on said bus.

145. (new) The apparatus of claim 144 wherein said bus is a PCI bus and said operations are type 1 control status register (CSR) cycles on said PCI bus.

146. (new) The apparatus of claim 95 further comprising

at least one incomplete transaction cache (ITC) with a sliding window, said sliding window having a width.

147. (new) The apparatus of claim 146 further comprising:

a delay mechanism configured to delay transmission of said cell responsive to a reduction of said width; and

a resumption mechanism configured to resume transmission of said cell responsive to an increase of said width.

148. (new) The apparatus of claim 146 further comprising a width adjustment mechanism configured to adjust said width responsive to receipt, at said first node, of said cell or a response cell.

149. (new) The apparatus of claim 95 further comprising:

a first cell generation mechanism at said first node configured to convert said bus operation into said cell;

a first cell transportation mechanism configured to transport said cell over said system interconnect from said first node to a second node; and

a bus operation mechanism at said second node configured to perform an equivalent bus operation on a second bus after receipt of said cell by said second node.

150. (new) The apparatus of claim 149 wherein the first cell generation mechanism further comprises:

an address mapping content addressable memory (AMCAM) responsive to said bus operation to determine an identifier for said first node; and

a cell address mechanism configured to include said identifier in said cell.

151. (new) The apparatus of claim 149 wherein said first bus is a first PCI bus and said second bus is a second PCI bus.

152. (new) The apparatus of claim 149 wherein said first bus is a PCI bus and said second bus is not.

153. (new) The apparatus of claim 149 further comprising:

a result acquisition mechanism at said second node configured to obtain a result from performance of said equivalent bus operation on said second bus;

a second cell generation mechanism at said second node configured to convert said result into a second cell;

a second cell transportation mechanism at said second node configured to transmit said second cell over said system interconnect from said second node to said first node; and

a bus operation completion mechanism at said first node configured to complete said bus operation on receipt of said second cell.

154. (new) The apparatus of claim 95 wherein said first node is a host node, and said apparatus further comprises:

a host node determination mechanism configured to determine whether said value identifies said host node; and

a broadcast mechanism configured to broadcast said cell when said value does not identify said host node.